42. The system of claim 41 wherein the MPEG Transport processor, the MPEG video decoder, the means for displaying the video and the system bridge controller are integrated on an integrated circuit chip.

43. The system of claim 41 wherein the MPEG video data include HDTV video data.

44. The system of claim 41 wherein the MPEG video data include SDTV video data.

REMARKS

Claims 1-44 remain in the present application. Claims 1, 22 and 41 have been amended. Applicants respectfully request reconsideration, reexamination and allowance of claims 1-44.

Applicants appreciate the Examiner's fully considering applicants' arguments mailed September 19, 2001 (which the Examiner refers to as "Applicant's arguments filed October 9, 2001"). However, applicants respectfully traverse the Examiner's finding that the claims of the present invention are not patentable over the cited references because of at least the following reasons.

A north bridge is typically used to interface between a CPU and a number of peripheral devices, such as, for example, I/O devices, a PCI bus, and system memory. The north bridge is typically implemented on a stand-alone integrated circuit chip, and the CPU as well as the peripheral devices are external to it. Thus, system integrators (e.g., PC board manufactures) typically have to use up board space for installing and connecting the north bridge between the external CPU and the external peripheral devices.

The present invention provides for a method and apparatus for integrating the north bridge function with a video and graphics system on an integrated circuit chip. For example, one embodiment of the present invention provides for "[a] system on an integrated circuit chip comprising: an MPEG video decoder for processing MPEG video data to generate video for displaying; means for displaying the video; and a system bridge controller having a north bridge function for coupling a CPU to a plurality of peripheral devices, wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip."

By integrating the north bridge function into the system bridge controller on an integrated circuit chip of a video and graphics system, the present invention provides further capabilities to the video and graphics system, namely, enabling CPU to interface with the peripheral devices, where both the CPU and the peripheral devices are situated outside the integrated circuit chip. Thus, the integrated circuit chip of the present invention has the added function of providing an interface capabilities to an external CPU, in addition to the video and graphics system functions of video decoding and displaying.

According to the Examiner, U.S. Patent No. 5,982,459 to Fandrianto et al.("Fandrianto") "teaches a system bridge controller for coupling a CPU to a plurality of peripheral devices when he discloses the pc processor connecting to an audio, video, and a camera (fig. 1 and 3-4; col. 3, lines 50-61; col. 5, lines 33-56)."

The Examiner further states that "Fandrianto teaches the RISC processor is a microprocessor (col. 5, lines 33-56). A microprocessor is a CPU. Therefore, the RISC processor connects to a plurality of peripheral devices such as an audio, video, and a camera (fig. 1 and 3). Thus, Fandrianto teaches a bridge

controller because he teaches the connections of a CPU to a plurality of peripheral devices."

However, applicants cannot find where in these figures and passages is a disclosure that a pc processor is connected to audio, video and a camera using a system bridge controller. For example, FIGs. 3 and 4 illustrate a block diagram of a RISC processor and a block diagram of a hardware coupled to a data bus used by a RISC processor, respectively. Applicants are not sure how these figures disclose the pc processor connecting to an audio, video, and a camera, thereby teaching a system bridge controller for coupling a CPU to a plurality of peripheral devices.

For further example, col. 3, lines 50-61 of Fandrianto recites, "A host interface 213 is for serial input and output of digital audio data. Audio interface 213 connects via a bus 113 to an audio DSP 160 and in one embodiment of the invention has IOM-2 (ISDN Oriented Modular Revision 2), MVIP (Multi-Vendor Integral Protocol), and CHI (concentration highway interface) bus capabilities. DSP 160 performs audio processing and controls audio input/output devices such as an audio codec 170 connected to a microphone 172 and a speaker 174," and does not discuss any north bridge function. Similarly, col. 5, lines 33-56 appears to discuss an instruction set for programming the RISC processor 220, and not a north bridge function provided by a system bridge controller.

Further, applicants respectfully submit that the RISC processor 220 of Fandrianto is not similar to the CPU in the claims of the present application for at least the following two reasons: 1) the RISC processor is implemented within the VCP 110 and not externally; and 2) the RISC processor is an integral part of an operation of the video processing by the VCP 110, and any communication between the RISC processor and other devices (audio,

video and camera) is appurtenant and incidental to its video and audio processing capabilities.

For example, "RISC processor 220 supervise hardware resources for input and output of compressed data, error correction and error correction coding, parsing bit streams, and interleaving audio and video data to form a bit stream" (col. 4, lines 21-24) in support of audio and video processing. Since the north bridge function of the system bridge controller in the present invention is in addition to any function it may have for video/audio processing, applicants respectfully submit that Fandrianto does not disclose a system bridge controller having a north bridge function. In other words, Fandrianto does not disclose a system bridge controller that connects an external CPU to external peripheral devices in a capacity as a north bridge.

Consider now the claims.

Claim 1 recites, in relevant portion, "a system bridge controller having a north bridge function for coupling a CPU to a plurality of peripheral devices, wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip."

Since Fandrianto does not teach or suggest a system bridge controller having a north bridge function for coupling a CPU to a plurality of peripheral devices, wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip, applicants respectfully request that the rejection to claim 1 be withdrawn and that claim 1 be allowed.

Since claims 2-21 depend, directly or indirectly, from claim 1, they incorporate all the terms and limitations of claim 1 in addition to other limitations, which together patentably distinguish them from the cited references. Therefore, applicants

respectfully request that the rejection to claims 2-21 be withdrawn and that they be allowed.

Claim 22 recites, in relevant portion, "coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function on an integrated circuit chip, wherein the integrated circuit chip is used to process MPEG video data to generate video for displaying and to display the video, and wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip."

Since Fandrianto does not teach or suggest coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function on an integrated circuit chip, wherein the integrated circuit chip is used to process MPEG video data to generate video for displaying and to display the video, and wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip, applicants respectfully request that the rejection to claim 22 be withdrawn and that claim 22 be allowed.

Since claims 23-40 depend, directly or indirectly, from claim 22, they incorporate all the terms and limitations of claim 22 in addition to other limitations, which together patentably distinguish them from the cited references. Therefore, applicants respectfully request that the rejection to claims 23-40 be withdrawn and that they be allowed.

Claim 41 recites, in relevant portion, "a system bridge controller having a north bridge function for coupling a CPU to at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and to a plurality of peripheral devices . . . wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip."

Since Fandrianto does not teach or suggest a system bridge controller having a north bridge function for coupling a CPU to at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and to a plurality of peripheral devices . . . wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip, applicants respectfully request that the rejection to claim 41 be withdrawn and that claim 41 be allowed.

Since claims 42-44 depend, directly or indirectly, from claim 41, they incorporate all the terms and limitations of claim 41 in addition to other limitations, which together patentably distinguish them from the cited references. Therefore, applicants respectfully request that the rejection to claims 42-44 be withdrawn and that they be allowed.

In view of the foregoing remarks, Applicants respectfully request allowance of claims 1-44. If the Examiner believes that a telephone conference with Applicants' attorney might expedite prosecution of the application, the Examiner is invited to call at the telephone number indicated below.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____
Jun-Young E. Jeon
Reg. No. 43,693
626/795-9900

JEJ/sd

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A system on an integrated circuit chip comprising:

an MPEG video decoder for processing MPEG video data to generate video for displaying;

means for displaying the video; and

a system bridge controller having a north bridge function for coupling a CPU to a plurality of peripheral devices,

wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip.

22. (Amended) A method of coupling a CPU to other devices comprising the steps of:

coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function on an integrated circuit chip,

wherein the integrated circuit chip is used to process MPEG video data to generate video for displaying and to display the video, and

wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip.

41. (Amended) A system comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data;

an MPEG video decoder for processing the MPEG video data to generate video for displaying;

means for displaying the video; and

a system bridge controller having a north bridge function for coupling a CPU to at least one of the MPEG Transport processor,

the MPEG video decoder and the means for displaying the video, and to a plurality of peripheral devices,

wherein the system bridge controller performs format conversion between big-endian data and little-endian data, between the CPU and at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and between the CPU and one or more of the plurality of peripheral devices,

wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip.

JEJ PAS414404.2-*-4/15/02 12:07 PM